Methods and Metrics for Reliability Assessment

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Abstract. This paper deals with digital VLSI design aspects related to reliability. The focus is on the problem of reliability evaluation in combinational logic circuits. We present some methods for this evaluation that can be easily integrated in a tradidional design flow. Also we describe suitable metrics for performance estimation of concurrent error detection schemes.

Keywords. Reliability, fault tolerance, combinational logic.

1 Introduction

The decreasing dimensions of electronic components allowed fabulous improvements in the services and products in a large variety of applications. An example of these are the wireless communications where computing power, mobility, compactness and power autonomy are major requirements. Nevertheless, as circuit dimensions decrease to nanometers, the amount of systematic, design-induced and parametric defects tends to increase. The production of perfect circuits is becoming economically prohibitive and, from now on, we must assume that the manufactured circuits can present defects or breakdowns [1, 2].

On the other hand, as circuits shrink, some of effects such as electrical and temporal masking are reducing. As a consequence, transient faults and soft error rates (SER) in combinational logic can no longer be considered negligible. SER per chip in logic circuits is expected to achieve the same orders of magnitude observed in unprotected memories [3].

The protection of memory elements that have a regular organization is fairly simple and do not impose critical overheads, but the protection of the logic parts in a circuit is generally associated with important overheads in terms of area, time or power. Fault-tolerant architectures, like the ones discussed in [4–6] have been historically targeted to mission critical applications, where reliability improvement and fault secureness are the main design objectives and the resulting overheads can be accepted.

With the expected reduction in the reliability of nanoscale CMOS, even ordinary circuits will need fault protection, but on these cases, the associated

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overheads must be minimized to guarantee some gain in the scaling process. To cope with these design constraints, i.e., reliability improvement and reduced overheads, partial fault tolerance and fault avoidance techniques are being considered. In all cases, the knowledge of the cost-quality trade-offs related to different approaches becomes crucial when choosing the reliability improvement scheme for a given design. With the reliability analysis integrated in the design flow, we are able to implement a closed-loop design process, with the reliability metric as a control parameter for the synthesis process.

This work deals with the problem of reliability evaluation in combinational logic circuits and the paper is organized as follows. Section 2 describes some approaches for reliability modelling. Metrics allowing comparison of concurrent error detection (CED) schemes are presented in section 3. Finally, in section 4, some conclusions and perspectives concerning reliability analysis are outlined.

2 Reliability Models

2.1 Reliability Modelling Based on PTM

Let be a logic circuit with m inputs and n outputs where each input can take value 0 or 1. The number of different combinations of input and output vectors is limited by 2^m and 2^n, respectively. Probabilistic Transfer Matrix (PTM) is defined as a matrix PTM where the $(i,j)^{th}$ entry represents the probability of output vector value j given input vector value i, i.e., $p(j \mid i)$ [7]. Therefore, PTM has 2^m rows and 2^n columns.

Figure 1 gives the example of PTM for OR logic gate. From the PTM matrix, we see that q is the probability of correct value and so $(1-q)$ is the probability of an error occurrence. For fault free gate, $q = 1$ so carrying to ideal transfer matrix (ITM).

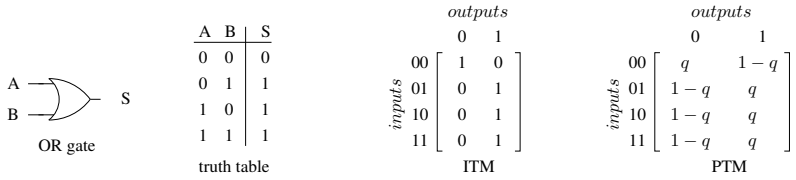

Fig. 1. Probabilistic transfer matrix (PTM) and ideal transfer matrix (ITM) for OR logic gate.

The PTM of a complex circuit is obtained by combining the PTM of the basic blocks with inner product or tensor product:

– If two gates G_1 and G_2 with PTM's P_{G_1} and P_{G_2} are combined in series, the resulting PTM is $P_{G_1} \times P_{G_2}$, that is, the inner product between the matrices.

– If two gates G_1 and G_2 with PTM's P_{G_1} and P_{G_2} are combined in parallel, the resulting PTM is $P_{G_1} \otimes P_{G_2}$, that is, the tensor product between the matrices.

The PTM approach allows the exact calculation of the error probabilities concerning logical masking. The logic masking of an error in a combinational circuit is the effect by which this error has no impact on the output value of this combinational function. In other words, given the other logical values present in the circuit (input values, internal values), the logical value of the node where the error occurred does not determine the value of the circuit output.

Given an input probability distribution, the reliability of the circuit can be modelled by using PTM and ITM, according to (1). In this expression, each $p(j|i)$ is a matrix element of the PTM, weighted by the probability of occurrence of corresponding input i.The (i, j) elements to be considered are those where the respective ITM matrix has a value of 1. It means that reliability is defined as the probability of a correct output.

$$R_{cir} = \sum_{ITM_{cir}(i,j)=1} p(j|i)p(i) \tag{1}$$

Reliability calculation based on PTM is accurate, but space and time complexities associated to the direct calculation of the PTM grow exponentially with the number of inputs and outputs so making this technique too expensive.

Efforts have been done to compress PTM representation using Algebraic Decision Diagrams (ADD's) [8], but these improvements do not help in reducing complexity for large circuit PTMs.

In order to address the scalability problem, Bhaduri *et al.* in [9] have proposed a script-based algorithm based on topological partitioning of the circuit. Nevertheless, the problem of memory still remains the bottleneck when stages have a large number of basic elements (gates and connections) in parallel.

We can observe that columns in intermediate PTM (especially from interconnections blocks) completely consist of zero values (see Fig. 2). Knowing what columns are non-zero avoids unnecessary calculations for PTM related to series association involving this kind of blocks. In [10], authors exploit this fact and propose a method to select the useful data for PTM calculation, so eliminating intermediate (and expensive) calculation of large order tensored PTMs.

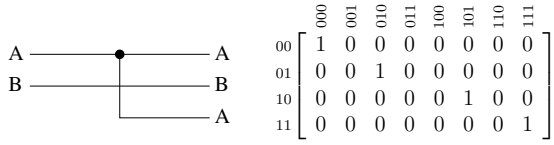

Fig. 2. Example of fault free wiring interconnection and its PTM.

Fig. 3 shows the circuit for a half-adder, where we can identify interconnection (S_0) and logic (S_1) blocks carrying to PTMs in Fig. 4. Notice that some columns of the matrix P_{S_0} completely consist of zero values. These columns have no influence on the calculation of global PTM $P_{HA} = P_{S_0 S_1} = P_{S_0} P_{S_1}$.

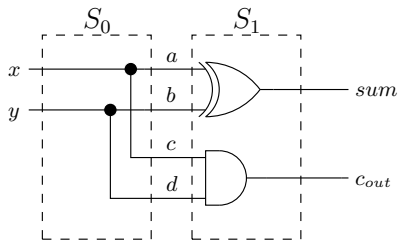

Fig. 3. Half-adder (HA) circuit.

Let the addressing of columns in P_{S_0} be from 0 to 15. According to this addressing, only the columns 0, 5, 10, 15 (in bold) are non-nulls and they correspond to the rows (also in bold) extracted from the P_{S_1} to form the total circuit probability transfer matrix P_{HA}. In Fig. 5 we can see that P_{HA} is a submatrix consisting of the useful rows in the matrix P_{S_1}.

2.2 Reliability Modelling Based on Logic Masking Coefficients

Consider a generic combinational logic circuit with input and output vectors $\mathbf{x}$ and $\mathbf{y}$, respectively. The reliability R_{cir} of such circuit can be determined as in (2), where $p(\mathbf{x})$ represents the probability of a given input $\mathbf{x}$ and $p(\mathbf{y} = correct|\mathbf{x})$ represents the probability that a correct output occurs given this input $\mathbf{x}$.

$$R_{cir} = \sum_{\text{for all } \mathbf{x}} p(\mathbf{x}) p(\mathbf{y} = correct|\mathbf{x}) \tag{2}$$

Denote y_i the output of the gate g_i. Consider that the occurrence of an error in a given gate results in an inversion of its output logic value. Define the **error vector** as the vector $\mathbf{e} = (e_1 e_2 \cdots e_w)$, where an element e_i is related to an error at gate g_i. Each e_i takes a value in $\{0, 1\}$ such that $e_i = 1$ means occurrence of error and $e_i = 0$ means good operation of the gate g_i in a circuit with w logic gates.

The amount of errors considered at a given moment in the target circuit is given by the number of $1's$ in vector $\mathbf{e}$. Denote the set of vectors $\mathbf{e}$ with k $1's$ by $\mathbf{e}_{w:k}$. This set contains C_k^w vectors, where C_k^w is the number of possible combinations of w elements taken k at a time given by $C_k^w = \frac{w!}{(w-k)!k!}$. These vectors represent all error vectors associated to k errors occurrence. With this notation, $\mathbf{e}_{w:0}$ is the particular case of a set with only one element, corresponding to an error-free circuit.

$$P_{S_0} = \begin{array}{c} \begin{matrix} \scriptstyle(0) & & & & & \scriptstyle(5) & & & & & \scriptstyle(10) & & & & & \scriptstyle(15) \end{matrix} \\ \begin{bmatrix} \mathbf{1} & 0 & 0 & 0 & 0 & \mathbf{0} & 0 & 0 & 0 & 0 & \mathbf{0} & 0 & 0 & 0 & 0 & \mathbf{0} \\ \mathbf{0} & 0 & 0 & 0 & 0 & \mathbf{1} & 0 & 0 & 0 & 0 & \mathbf{0} & 0 & 0 & 0 & 0 & \mathbf{0} \\ \mathbf{0} & 0 & 0 & 0 & 0 & \mathbf{0} & 0 & 0 & 0 & 0 & \mathbf{1} & 0 & 0 & 0 & 0 & \mathbf{0} \\ \mathbf{0} & 0 & 0 & 0 & 0 & \mathbf{0} & 0 & 0 & 0 & 0 & \mathbf{0} & 0 & 0 & 0 & 0 & \mathbf{1} \end{bmatrix} \end{array}$$

$$P_{S_1} = \begin{array}{c} \begin{matrix} & \scriptstyle(0) & \scriptstyle(1) & \scriptstyle(2) & \scriptstyle(3) \end{matrix} \\ \begin{matrix} \scriptstyle(0) \\ \\ \\ \\ \\ \scriptstyle(5) \\ \\ \\ \\ \\ \scriptstyle(10) \\ \\ \\ \\ \scriptstyle(15) \end{matrix} \begin{bmatrix} \mathbf{q^2} & \mathbf{qp} & \mathbf{pq} & \mathbf{p^2} \\ q^2 & qp & pq & p^2 \\ q^2 & qp & pq & p^2 \\ qp & q^2 & p^2 & pq \\ pq & p^2 & q^2 & qp \\ \mathbf{pq} & \mathbf{p^2} & \mathbf{q^2} & \mathbf{qp} \\ pq & p^2 & q^2 & qp \\ p^2 & pq & qp & q^2 \\ pq & p^2 & q^2 & qp \\ pq & p^2 & q^2 & qp \\ \mathbf{pq} & \mathbf{p^2} & \mathbf{q^2} & \mathbf{qp} \\ p^2 & pq & qp & q^2 \\ q^2 & qp & pq & p^2 \\ q^2 & qp & pq & p^2 \\ q^2 & qp & pq & p^2 \\ \mathbf{qp} & \mathbf{q^2} & \mathbf{p^2} & \mathbf{pq} \end{bmatrix} \end{array}$$

Fig. 4. PTM for wiring interconnections and logic in a HA.

$$P_{HA} = \begin{bmatrix} q^2 & qp & pq & p^2 \\ pq & p^2 & q^2 & qp \\ pq & p^2 & q^2 & qp \\ qp & q^2 & p^2 & pq \end{bmatrix}$$

Fig. 5. PTM for the complete half-adder.

Considering distinct reliability values q_i for each gate, the reliability of the circuit can be described by (3) with a PBR (Probabilistic Binomial Reliability) model [11]. This assumes that the error distribution is independent among all the gates. In this expression, $\mathbf{x}_j$ denotes the j-th input vector $\mathbf{x}$, represented by the binary code of j. Consider that input consists of m input logic values (m-bit vector). With $m = 3$ and $j = 5$, $\mathbf{x}_5$ corresponds to the input vector (101). In the same way, $\mathbf{e}(s)$ denotes the s-th error vector $\mathbf{e}$, represented by the binary code of s. For example, with $w = 4$ and $s = 5$, $\mathbf{e}(5)$ corresponds to the error vector (0101) and so to $k = 2$ errors.

The term $\overline{y(\mathbf{x}_j, \mathbf{e}(0)) \oplus y(\mathbf{x}_j, \mathbf{e}(s))}$ represents the masking test based on complemented exclusive-or logic function. For a given input vector $\mathbf{x}_j$, it compares the output y resulting of a error-free circuit (i.e. considering $\mathbf{e}(0)$) with the output y of this same circuit under a given error configuration $\mathbf{e}(s)$. When both outputs are identical, it returns 1 and means that $\mathbf{e}(s)$ is masked, provided that it occurs when input vector is $\mathbf{x}_j$.

$$R_{cir} = \sum_{s=0}^{2^w-1} \prod_{correct} q_i \prod_{incorrect} (1-q_i) \sum_{j=0}^{2^m-1} p(x_j) \left(\overline{y(\mathbf{x}_j, \mathbf{e}(0)) \oplus y(\mathbf{x}_j, \mathbf{e}(s))} \right) \quad (3)$$

Assuming uniform probability distribution for input vectors $\mathbf{x}$ and same identitical q for all gates in the circuit, the reliability function can be simplified as in (4), where $\breve{c}_k$ is given as in (5) and function $f(q)$ is given by the expression $f(q) = (1-q)^k q^{w-k}$.

$$R_{cir} = \frac{1}{2^m} \sum_{k=0}^{w} f(q) \, (\breve{c}_k) \quad (4)$$

$$\breve{c}_k = \sum_{l=1}^{C_k^w} \sum_{j=0}^{2^m-1} \overline{y(\mathbf{x}_j, \mathbf{e}_{w:0}) \oplus y(\mathbf{x}_j, \mathbf{e}_{w:k}(l))} \quad (5)$$

The coefficients $\breve{c}_k$ serve as parameters in R_{cir} related to the logical masking of the circuit against k errors and can be used to different tradeoffs between complexity and accuracy of R_{cir}. Because of the assumed independence, the amount of errors in a given time $P(k, w)$ can be modeled as a binomial distribution when gates have the same reliability q.

$$P(k, w) = (C_k^w) q^{w-k} (1-q)^k \quad (6)$$

The relevant range of error probabilities in a circuit results from several parameters like particle hit rate, density of logic gates, voltage operation, etc. In this way, the range of q values becomes an input parameter for the PBR model. The knowledge or specification of this range of values allows to reduce the overall complexity for reliability calculation. Supposing that the designer is interested

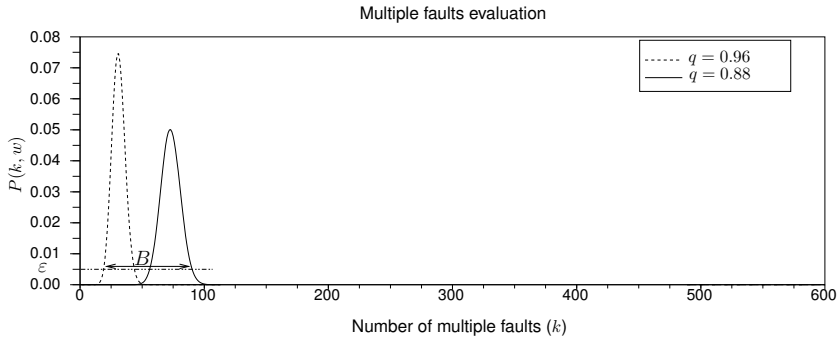

Fig. 6. Multiple faults analysis for coefficients determination.

on the circuit reliability in the range $0.88 < q < 0.96$ and that the circuit has 600 gates, Fig. 6 shows the probabilities of multiple errors in the desired range.

The ε bound in Fig. 6 represents the expected multiple faults probabilities that can be considered negligible in the design. This bound is another useful information for complexity reduction because it puts in evidence the coefficients that are effectively important in the reliability calculation.

The smaller the value of ϵ chosen by the designer, the better is the accuracy of the function in the desired range. For the presented example, with $\epsilon = 0.005$, the coefficients to be computed are the ones over the range B, that is, $\breve{c}_{20}$ to $\breve{c}_{81}$. This reduced order reliability function and the exact curve computed with all coefficients are compared in Fig. 7.

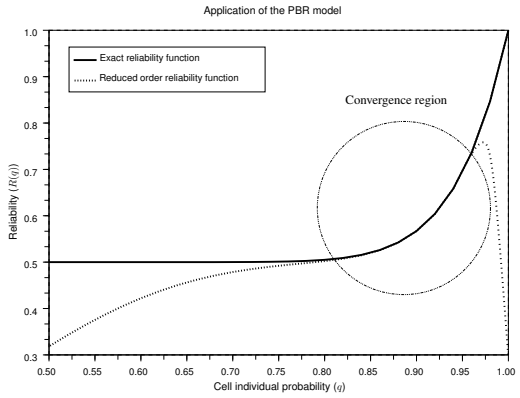

Fig. 7. Full PBR model results compared with a relaxed PBR model.

2.3 Reliability Modelling Based on Signal Probability

Reliability of a given circuit can be computed on the basis of the cumulative effect of errors in the signals of the circuit. The algorithm SPRA (Signal Probability Reliability Analysis) described in [12] takes into account the gates/cells failure probability and the topological structure of circuit to determine the probability of correctness of the signals. The cumulative effect of errors embeds the contribution of multiple simultaneous faults to the reliability of the circuit.

The main difference of the proposed method to other signal probabilities approaches is the explicit representation of the four possible states of a fault-prone binary signal. Besides the probabilities of occurrence of 0 and 1, the four-state probability representation includes the probabilities of occurrence of incorrect 0 and 1. An incorrect 0 is a value that should be 1 in a fault-free condition, and an incorrect 1 is a value that should be a 0 in a fault-free condition. Fig. 8 shows this matrix representation.

$$signal = \begin{bmatrix} 0_{correct} & 1_{incorrect} \\ 0_{incorrect} & 1_{correct} \end{bmatrix}$$

(a)

$$P_{2\times 2}(signal) = \begin{bmatrix} P(0_{correct}) & P(1_{incorrect}) \\ P(0_{incorrect}) & P(1_{correct}) \end{bmatrix}$$

(b)

Fig. 8. Matrix representation of (a) the four-state signal and (b) associated probabilities.

The four-state signal probability embeds the reliability information of a given signal, since it can be obtained by computing its probability of correctness, i.e.,

$$R_{signal} = P(0_{correct}) + P(1_{correct})$$

The signal probabilities for the nodes in a circuit can be obtained by propagating the input probabilities through the gates of the circuit. The propagation process uses the probability of failure of a given gate and its input signal probabilities to compute the output signal probabilities.

The probability of failure of a gate is represented by a probabilistic transfer matrix (PTM) and its fault-free function is represented by an ideal transfer matrix (ITM) as described in section 2.1. The input signal probabilities (I) of a given gate can be determined by the joint probability (tensor product, Kronecker product) of its input signals.

The output signal probabilities of a gate can be determined by the multiplication of the input signal probabilities by the PTM of the gate, according to (7) and (8). Figure 9 illustrates the reliability calculation for an OR gate based on this method.

$$I_{gate} = input(1) \otimes input(2) \otimes .. \otimes input(n) \tag{7}$$

$$P(S) = I_{gate} \times PTM_{gate} \tag{8}$$

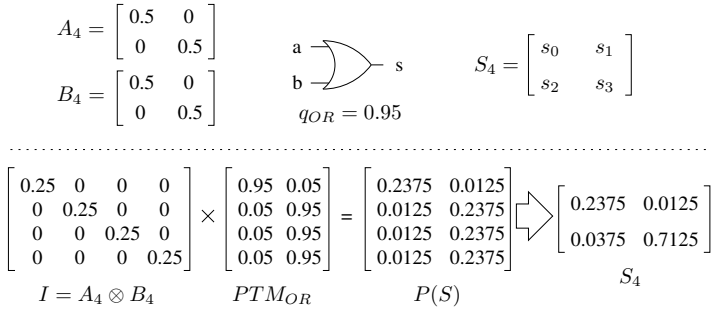

Fig. 9. Signal probability propagation in an OR gate.

Once the probabilities of the output signals have been determined by the propagation process, the reliability of the circuit can be computed by multiplying the reliability of the output signals. This algorithm computes the exact value of signal reliability of circuit with no fanout nodes. In the presence of signal correlations, a multi-pass algorithm is required. Considering that each fanout signal has four possible states, the multi-pass algorithm computes the contribution of each state of each fanout node to the reliability of the circuit and the addition of all these contributions gives the exact reliability of the circuit, as in (9), where f is the number of fanouts in the circuit and j represents the $j-th$ iteration of the algorithm.

$$R = \sum_{j=1}^{k=2f} R(j) \tag{9}$$

The scalability of the multi-pass algorithm is dependent of the number of fanout nodes in the circuit, and a tradeoff between accuracy and processing time is possible by taking into account a reduced number of fanout signals. A small error margin is still possible when computing the reliability based on a reduced number of fanouts.

Also, to avoid unnecessary calculations, each iteration step can propagate only the signal probabilities related to the fanout signal whose state has been updated. Furthermore, propagations related to null state probability can be skipped. The algorithm presents no memory bottlenecks since only the signal probability matrices for the current propagation step must be stored.

3 Reliability Analysis of Concurrent Error Detection Schemes

Consider the general architecture of a system with concurrent error detection in a multiple fault environment as shown in Fig. 10. The possible output events in such assembly are defined as follows.

- ξ : the checker circuit indicates a valid operation when the circuit outputs are correct.
- τ : the checker circuit indicates a non-valid operation when the circuit outputs are correct.
- ψ : the checker circuit indicates a valid operation when the circuit outputs are incorrect.
- χ : the checker circuit indicates a non-valid operation when the circuit outputs are incorrect.

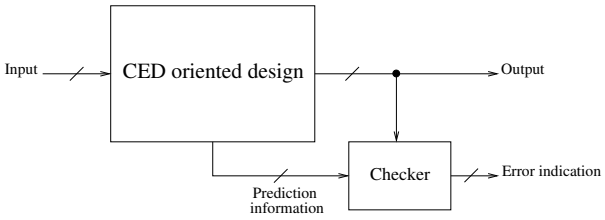

Fig. 10. General CED scheme

Define the *effective reliability* $\Re$ of the system by the conditional probability in (10), where the ψ event represents the event associated with the non-detected errors and $\Re$ takes into account the correct outputs given that the checker indicated correct operation.

$$\Re = p\,(\xi | \xi \cup \psi) \tag{10}$$

The *time penalty* Γ can be defined as the probability of the events union τ and χ as given in (11). This probability has a direct impact in the effective throughput of the global system which the CED scheme is embedded. The higher is the value of Γ, the lower is the number of valid data propagated to next stage per time unit.

$$\Gamma = p\,(\tau \cup \chi) \tag{11}$$

The framework shown in Fig. 11 is considered in order to compute the probabilities defined in previous paragraphs. The dashed modules in the figure are fault free versions and work concurrently with the scheme under analysis. To ensure accuracy in the analysis, an exhaustive functional simulation of the system

should be done. The idea is to submit the CED design under analysis to every possible multiple fault prone and verify the output pair (f_i,v_i) for each possible input vector.

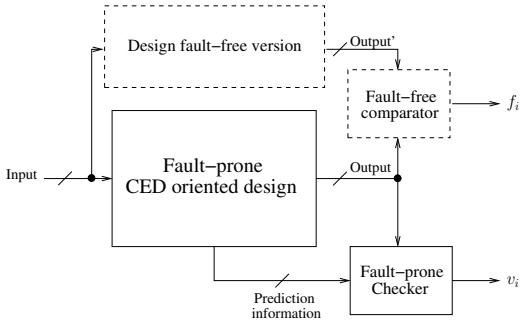

Fig. 11. Proposed framework.

The events ξ, τ, ψ and χ are associated with the state of the pair (f_i,v_i) and equalities in Fig. 12 are verified:

- $f_i = 1$ when the output of the CED scheme under analysis is really correct and $f_i = 0$ otherwise,
- $v_i = 0$ when the checker indicates non-valid operation and $v_i = 1$ for a valid one[1].

$$\begin{cases} p(f_i = 1, v_i = 1) = p(\xi) \\ p(f_i = 1, v_i = 0) = p(\tau) \\ p(f_i = 0, v_i = 1) = p(\psi) \\ p(f_i = 0, v_i = 0) = p(\chi) \end{cases}$$

Fig. 12. Defining probabilities for output events.

The desired probabilities can be computed as (12), (13), (14) and (15). It assumes that the inputs are uniformely distributed and considers PBR model given in section 2.2, where $f(q,k) = (1-q)^k.q^{w-k}$ and the coefficients α_k, β_k, γ_k and δ_k are associated with the occurence of the pairs $(f_i = 1, v_i = 1)$, $(f_i = 1, v_i = 0)$, $(f_i = 0, v_i = 1)$, $(f_i = 0, v_i = 0)$, respectively.

[1] Since two-rail checkers have two outputs (g and h) we code them in an one bit representation $v_i = g \oplus h$, where $\oplus$ is the exclusive-OR operation.

$$E(q) = \frac{1}{2^m} \sum_{k=0}^{w} f(q,k)\alpha_k \tag{12}$$

$$T(q) = \frac{1}{2^m} \sum_{k=0}^{w} f(q,k)\beta_k \tag{13}$$

$$U(q) = \frac{1}{2^m} \sum_{k=0}^{w} f(q,k)\gamma_k \tag{14}$$

$$X(q) = \frac{1}{2^m} \sum_{k=0}^{w} f(q,k)\delta_k \tag{15}$$

Therefore, the *effective reliability* $\Re(q)$ and the *time penalty* $\Gamma(q)$ are calculated as shown in (16) and (17). The knowledge of $\Re$ and Γ is quite useful in an analysis to decide which fault tolerant approach to choose. $\Re$ can be directly compared with the reliability measure from others solutions, like error masking schemes such TMR and NAND-Multiplexing techniques [13]. Adding up the information provided by Γ one can completely characterize the CED scheme to better evaluate the tradeoffs involved.

$$\Re(q) = \frac{E(q)}{E(q) + U(q)} \tag{16}$$

$$\Gamma(q) = T(q) + X(q) \tag{17}$$

We have evaluated the intrinsic time penalty of two-rail checkers. Two-rail checkers are widely used in concurrent error detection schemes such as duplication and parity prediction. It consists in a circuit that has two groups of inputs $(z_0, z_1, ..., z_n)$ and $(z2_0, z2_1, ..., z2_n)$ and two outputs g and h. If every pair z_j, $z2_j$ is complementary for all $j = 0, 1, 2, ...n$, the outputs should be also complementary. These kind of checkers are totally self checking for all single and unidirectional multiple faults [5]. The information that in general is not considered is how representative is the rate of false indications when correct complementary inputs z_j, $z2_j$ occur. It relies on the computation of $T(q)$. By applying uniformely distributed complementary inputs, we evaluated the behavior of $T(q)$ for single and multiple faults separately as the depth of the tree increases. The curves are shown in Fig. 13 as function of the individual gate failure probability $1 - q$.

We also considered the problem of which concurrent error detection scheme to choose for arithmetic operators. Three different CED schemes have used in a 4-bit ripple-carry adder: a fault-secure parity prediction adder [4], an identical duplex scheme [6] and a diverse duplex one. Since gate failure probabilities are independent, all possible multiple faults are contemplated and its occurence probability is described by a binomial random variable. The curves of effective reliability $\Re(q)$ and time penalty $\Gamma(q)$ are showed as a direct function of q in Fig. 14 and Fig. 15, respectively.

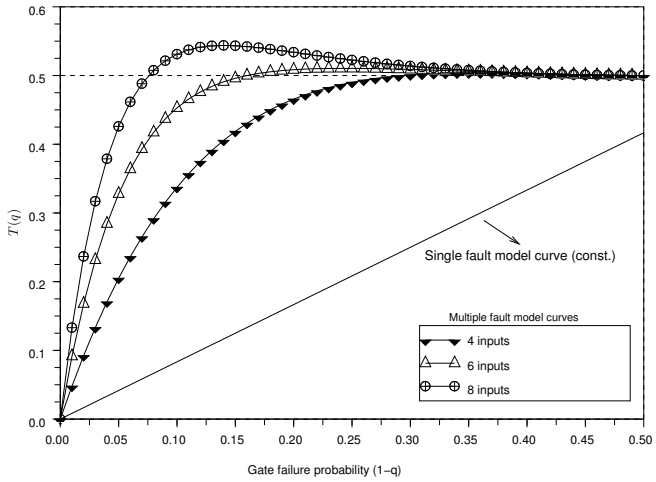

Fig. 13. Two-rail checker tree: time penalty evaluation.

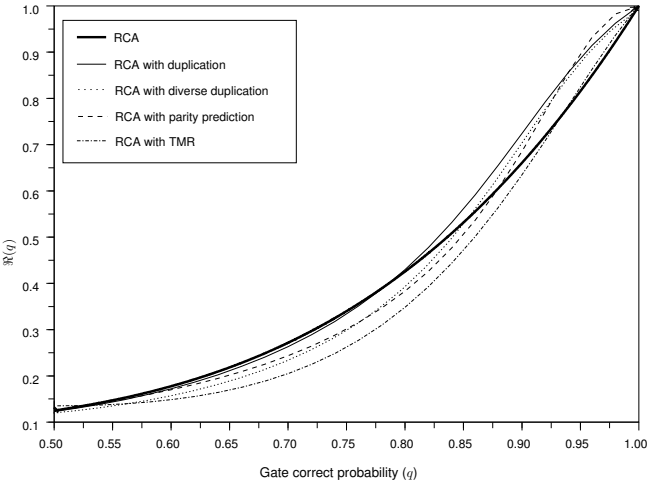

Fig. 14. Effective reliability $\Re(q)$.

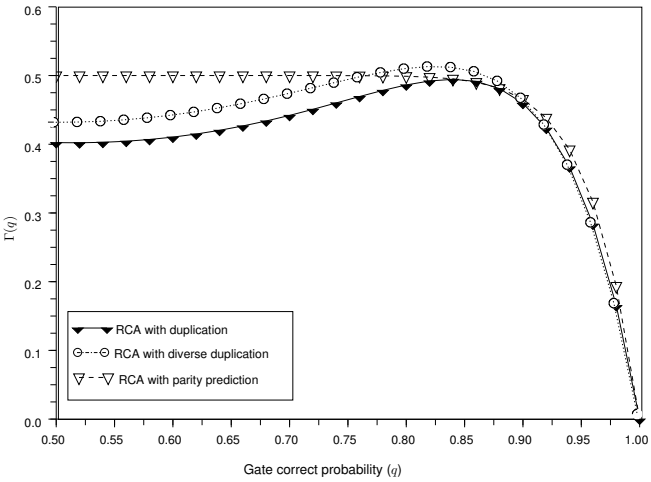

Fig. 15. Time penalty $\Gamma(q)$.

4 Conclusions

Reliability is becoming a major concern for semiconductor companies and circuit designers. Reliability improvement can be obtained with fault prevention, by improving the intrinsic reliability of the circuit and its components. The reliability of individual logic cells is the main focus of fault prevention techniques. On the other hand, fault-tolerant architectures act in the upper level, improving reliability related to the topological structure of the circuit. All of these solutions represent tradeoffs between area, power consumption, operating frequency and reliability. At the heart of these techniques there's a need for accurate and fast reliability analysis tools, that could be embedded in the design flow, being transparent to the designer.

This paper addressed the problem of estimating the reliability with presentation of some methods to calculate reliability of combinational circuits and metrics to evaluate reliability of concurrent error detection schemes. The PBR model described in 2.2 is a method that allows the determination of the analytical equation for the reliability of the target circuit. With the reliability equation available, many types of analysis can be done, like the susceptibility of the circuit to single and multiple faults, the reliability of the circuit for any particular value of individual gates reliability, among others. Also, the possibility of straightforward application of the method SPRA described in section 2.3 make it a good candidate for a integrated estimation of reliability in the design process of ASIC circuits.

This integration would allow the synthesis tool to directly choose the adequate cells from the library, among functionally equivalent ones, according to the specified design constraints. We are continuing our studies on reliability and

further work concerns the evaluation of other signal correlation heuristics and the incorporation of electrical and temporal masking in the proposed analysis.

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